S.E. Extc Sem IV 26 May '201
Analog & digital IC Design & Application

Con. 3323–10. (REVISED COURSE) AN–3484

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data if **required**.

1. (a) Explain the following term in relation to PLL :– 5
   (i) Lock range
   (ii) Capture range.
   (b) Explain switch Debouncing with circuit diagram. 5
   (c) Explain following term with reference to DAC. 5
   (i) Linearity
   (ii) Resolution
   (iii) Accurancy.
   (d) Compare active filter and passive filter. 5

2. (a) Obtain the transfer function for KRC low pass filter and draw the circuit. Calculate the component value if f_0 = 2 kHz. and Q = 4. 10
   (b) Explain VCO IC 566 and its features. 10

3. (a) Explain Monostable multivibrator using IC 555 with the internal circuit diagram of IC 555, draw the wave form. Calculate the value of R and C for pulse width of 20 ms. 10
   (b) What are the performance parameters of DAC. Explain any one technique of DAC. 10

4. (a) What is Instrumentation amplifier, explain it with three opamp, and write down advantages and disadvantages of it. 10
   (b) Explain opamp as voltage to current converter and mention the application of V-I converter. 10

5. (a) Design a Moore machine for overlap sequence detector for the string "1110". The output must be '1' when the input matches this string – 10
   (i) Draw the state diagram
   (ii) Write its transition and output table
   (iii) Draw its Logic diagram.
   (b) Draw and explain the block diagram of FPGA. 10

6. (a) Write VHDL code for a four bit up counter. 8
   (b) A fundamental-mode circuit is to have two inputs and a single output, which becomes '1' only upon the ocurrance of the last in the following sequence of input combination, otherwise z = 0. 12
   x_1 x_2 : 0 0 0 1 1 1 1 0
   Construct primitive flow table.

7. Write short notes (any **three**) :– 20
   (a) Structural Modelling
   (b) Races and Cycles
   (c) Compare Static and Dynamic RAM
   (d) Log Amplifier.